INTEGRATED CIRCUITS
UNITRODE

UC1710
UC3710

High Current FET Driver

FEATURES

- Totem Pole Output with 6A Source/Sink Drive
- 5ns Delay
- 5ns Rise and Fall Time into 2.2nF
- 5ns Rise and Fall Time into 30nF
- 4.7V to 18V Operation
- Inverting and Non-Inverting Outputs
- Under-Voltage Lockout with Hysteresis
- Thermal Shutdown Protection
- MINIDIP and Power Packages

DESCRIPTION

The UC1710 family of FET drivers is made with a high-speed Schottky process to interface between low-level control functions and very high-power switching devices-particularly power MOSFET's. These devices accept low-current digital inputs to activate a high-current, totem pole output which can source or sink a minimum of 6A.

Supply voltages for both V_{IN} and V_C can independently range from 4.7V to 18V. These devices also feature under-voltage lockout with hysteresis.

The UC1710 is packaged in an 8-pin hermetically sealed dual in-line package for -55°C to +125°C operation. The UC3710 is specified for a temperature range of 0°C to +70°C and is available in either an 8-pin plastic dual in-line or a 5-pin, TO-220 package. Surface mount devices are also available.

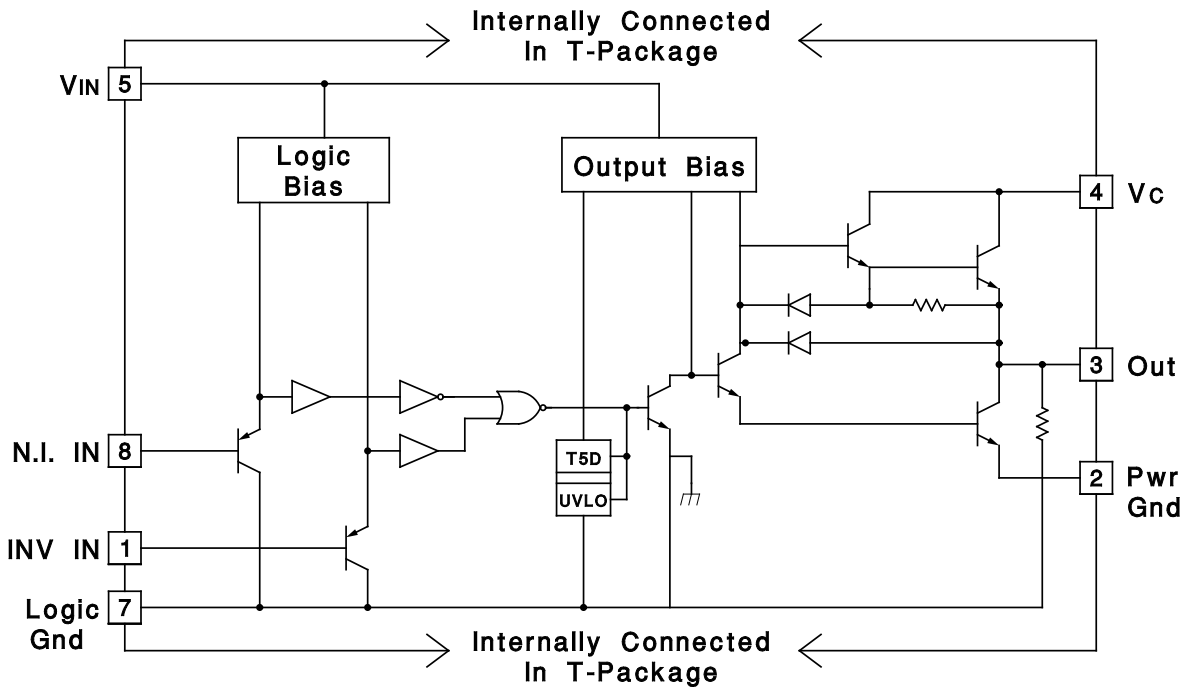
TRUTH TABLE

INV	N.I.	Out
H	H	L
L	H	H
H	L	L
L	L	L

OUT= $\overline{\text{INV}}$ and N.I.

$\overline{\text{OUT}}$= INV or $\overline{\text{N.I.}}$

BLOCK DIAGRAM



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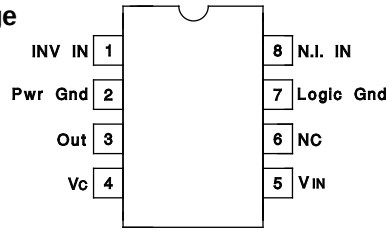
ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg	T-Pkg
Supply Voltage, Vin	20V	20V	20V
Collector Supply Voltage, V_C	20V	20V	20V
Operating Voltage	18V	18V	18V
Output Current (Source or Sink)			
Steady-State	±500mA	±500mA	±1A
Digital Inputs	-0.3V-V_{IN}	-0.3V-V_{IN}	-0.3V-V_{IN}
Power Dissipation at Ta=25°C	1W	1W	3W
Power Dissipation at T (Case) = 25°C	2W	2W	25W
Operating Junction Temperature	-55°C-+150°C	-55°C-+150°C	-55°C-+150°C
Storage Temperature	-65°C-+150°C	-65°C-+150°C	-65°C-+150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

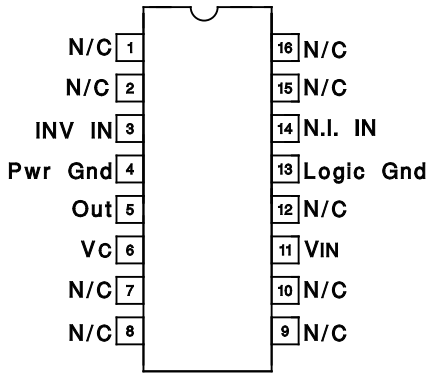
Note 1: All currents are positive into, negative out of the specified terminal.
Note 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

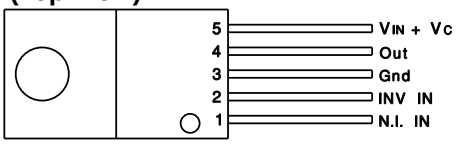
DIL-8 MINIDIP (Top View)
J or N Package



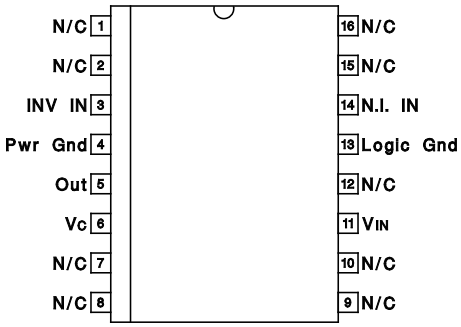
DIL-16 (Top View)
SP Package



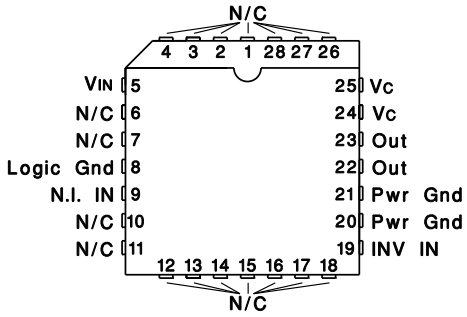
5-Pin TO-220 (Top View)
T Package



SOIC-16 (Top View)
DW Package



PLCC-28 (Top View)
QP Package



ELECTRICAL CHARACTERISTICS:

(Unless otherwise stated, these specifications apply for T_A =- 55°C to +125°C for the UC1710 and T_A = 0 °C to +70°C for the UC3710; V_{IN} = Vc = 15V, No load T_A = T_J.)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	V_{IN}=18V, Vc=18V, Output Low		26	35	mA
	V_{IN}=18V, Vc=18V, Output High		21	30	mA
Vc Supply Current	V_{IN}=18V, Vc=18V, Output Low		1.5	5.0	mA
	V_{IN}=18V, Vc=18V,Output High		5.0	8	mA
UVLO Threshold	V_{IN} High to Low	3.8	4.1	4.4	V
	V_{IN} Low to High	4.1	4.4	4.8	V
UVLO Threshold Hysteresis		0.1	0.3	0.5	V
Digital Input Low Level				0.8	V
Digital Input High Level		2.0			V

ELECTRICAL CHARACTERISTICS (cont.)

(Unless otherwise stated, these specifications apply for T_A =- 55°C to +125°C for the UC1710 and T_A = 0 °C to +70°C for the UC3710; V_{IN} = Vc = 15V, No load. $T_A = T_J$.)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input Current	Digital Input=0.0V	-70	-4.0		µA
Output High Sat., Vc-Vo	Io=-100mA		1.35	2.2	V
	Io=-6A		3.2	4.5	V
Output Low Sat., Vo	Io = 100mA		0.25	0.6	V
	Io = 6A		3.4	4.5	V
Thermal Shutdown			165		°C
From Inv.,Input to Output (Note 3, 4):					
Rise Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	70	ns
10% to 90% Rise	CL = 0		20	40	ns
	CL = 2.2nF		25	40	ns
	CL = 30nF		85	150	ns
Fall Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	80	ns
90% to 10% Fall	CL = 0		15	40	ns
	CL = 2.2nF		20	40	ns
	CL = 30nF		85	150	ns
From N.I. Input to Output (Note 3,4):					
Rise Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	70	ns
10% to 90% Rise	CL = 0		20	40	ns
	CL = 2.2nF		25	40	ns
	CL = 30nF		85	150	ns
Fall Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	80	ns
90% to 10% Fall	CL = 0		15	40	ns
	CL = 2.2nF		20	50	ns
	CL = 30nF		85	150	ns

Note: 3. Delay measured from 50% input change to 10% output change.
Note: 4. Those parameters with CL = 30nF are not tested in production.
Note: 5. Inv. Input pulsed at 50% duty cycle with N.I. Input = 3V. or N.I. Input pulsed at 50% duty cycle with Inv. Input = 0V.

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